

**This Page Is Inserted by IFW Operations
and is not a part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- **BLACK BORDERS**
- **TEXT CUT OFF AT TOP, BOTTOM OR SIDES**
- **FADED TEXT**
- **ILLEGIBLE TEXT**
- **SKEWED/SLANTED IMAGES**
- **COLORED PHOTOS**
- **BLACK OR VERY BLACK AND WHITE DARK PHOTOS**
- **GRAY SCALE DOCUMENTS**

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

UNITED STATES PATENT APPLICATION

FOR

FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF

Inventors:
Hao Fang
Yue-Song He
Mark S. Chang
Kent K. Chang

Sawyer Law Group LLP
2465 East Bayshore Road, Suite 406
Palo Alto, California 94303

0944370-082801

FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF

FIELD OF THE INVENTION

The present invention relates to flash memory devices, and more particularly to a method for fabricating a flash memory device.

BACKGROUND OF THE INVENTION

A flash memory device typically includes a core area and a periphery area. The core area includes memory transistors, while the periphery area contains both low-voltage transistors for handling logic and switching circuitry, and high-voltage transistors for handling high-voltages encountered during flash memory programming and erase operations.

Figure 1 is a top view of a portion of a conventional NAND flash memory device 10. The flash memory device 10 includes a core area 12 and a periphery area 14. The core area 12 includes an array of memory transistors 16 and two select gate regions that include a row of select transistors connected by a select word-line 28. One select gate region is referred to as a select drain gate region 18 and the other select gate region is referred to as a select source gate region 20. Although not shown, the periphery area 14 contains low-voltage transistors for handling logic and switching circuitry, and high-voltage transistors for handling high-voltages encountered during flash memory programming and erase operations.

The memory transistors 16 are stacked gate structures that include a layer of type-1 polysilicon (poly1) 22 that form floating gates, and a layer of type-2 polysilicon (poly2) that forms word-lines 26 interconnecting a row of memory transistors 16. The select transistors

in the select gate regions 18 and 20 are single gate structures comprising a layer of poly1 22, which also forms the select word-line 28 connecting the select gate transistors. Fabricating such an device is a multi-step process.

Figure 2 is a flow chart illustrating conventional process steps required to fabricate a flash memory device 10. Also shown is a series of cross sectional views (Figures 2(a-g)) of a substrate showing the resulting structure.

First a dual core gate oxide is performed, via step 40. Typically a dual core gate oxide is implemented to fabricate oxide layers of different thickness in the core area. Next, a nitridation process is performed, via step 42. This is done to improve the reliability of the core gate oxide. Typically, the nitridation process involves the introduction of nitrogen to the Si-SiO₂ interface in the core and periphery areas. Next, a layer of type-1 polysilicon (poly1) is deposited in both the core area and periphery area, via step 44. After the poly1 is patterned, a layer of oxide nitride oxide (ONO) is deposited over the poly1 layer, via step 46.

After the layer of ONO is deposited, the core area is covered by photo resist and the ONO and poly1 layer is removed in the periphery area, via step 48. Then, a dual periphery gate oxide is performed, via step 50. Finally, a type-2 layer of polysilicon (poly2) is deposited in all areas and the gate stacks are formed, via step 52.

As previously mentioned, a nitridation process is performed after the dual core gate oxide in order to improve the reliability of the core gate oxide. However, when the

nitridation process is performed, nitrogen is also introduced in the periphery area. Because the presence of nitrogen residue in the periphery area inhibits the subsequent growth of oxide in the periphery area, the quality of the dual periphery gate oxide is problematic based on the existence of defects related to the nitrogen residue.

Consequently, the nitrogen contamination problem is a technically difficult issue that hinders the implementation of nitridation in the flash memory fabrication process.

Therefore, the reliability of the core gate oxide and thus the reliability of the flash memory device, becomes more of a concern. Several techniques, such as reoxidation treatment after nitridation or using a hard mask to cover the periphery area during nitridation have been used. However, these methods complicate the process and introduce some side effects as well.

Accordingly, an improved method of fabricating a flash memory device is needed. The method should be cost effective, easy to implement and shouldn't add undue complexity to existing fabrication methods. The present invention addresses such a need.

SUMMARY OF THE INVENTION

In a first aspect of the present invention, a method of fabricating a flash memory device is disclosed. The method comprises the steps of providing a portion of a dual gate oxide in a periphery area of the memory device and then simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area. Finally, a nitridation process is provided in both the core and periphery areas subsequent to the previous steps.

In a second aspect of the present invention, a flash memory device is disclosed. The flash memory device comprises a core area having a plurality of memory transistors comprising an oxide layer, a first poly layer, an interpoly dielectric layer, and a second poly layer. The flash memory device further comprises a periphery area having a plurality of

transistors comprising an oxide layer, a portion of the first poly layer, and the second poly layer.

According to the present invention, the use of the method for fabricating the flash memory device results in a significant improvement in the oxide reliability in the core and periphery areas and also eliminates the nitrogen contamination problem in the periphery area.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a top view of a portion of a conventional NAND flash memory device.

Figure 2 is a flow chart illustrating conventional process steps required to fabricate a conventional flash memory device as well as a series of cross sectional views of a substrate showing the resulting structure.

Figure 3 is a flow chart illustrating the processing steps for fabricating a NAND flash memory device according to a preferred embodiment of the present invention as well as a series of cross sectional views of the resulting structure at the corresponding process steps.

Figure 4 is an exploded view of Figure 3(g) illustrating a cross sectional view of a flash memory device in accordance with present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to an improvement in the fabrication of flash memory devices. The following description is presented to enable one of ordinary skill in the art to

make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be grown to other embodiments. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

A preferred embodiment of the present invention provides a NAND flash memory device and a method for fabricating the same. Utilizing a method in accordance with the present invention, the dual periphery gate oxide is provided first and the nitridation process is provided subsequent to providing the dual periphery gate oxide. By providing the nitridation process subsequent to providing the dual periphery gate oxide, the dual periphery gate oxide can be provided in a less difficult fashion since it is easier to grow oxide when there is no nitrogen present. Furthermore, as a result of providing the nitridation process subsequent to providing the dual periphery gate oxide, the reliability of the flash memory is improved.

Figure 3 is a flow chart illustrating the processing steps for fabricating a NAND flash memory device according to a preferred embodiment. Also shown is a series of cross sectional views (Figures 3(a-g)) of a substrate showing the resulting structure.

The process begins by providing a portion of a dual periphery gate oxide, via step

200. Next, a dual core gate oxide is provided, along with the completion of the dual periphery gate oxide, via step 202. A nitridation process is then provided, via step 204.

By providing the nitridation process after forming the dual periphery gate oxide and the dual core gate oxide, the reliability of the flash memory device is significantly improved

over flash memory devices formed by a conventional process.

Referring back to Figure 3, next, a layer of type-1 polysilicon (poly1) is deposited in both the core area and periphery area, via step 206. After the poly1 is patterned, a layer of oxide nitride nitride (ONO) is deposited over the poly1 layer, via step 208. After the layer of ONO is deposited, the core area is covered by photo resist and the ONO layer, along with a portion of the poly1 layer is removed in the periphery area, via step 210.

In a preferred embodiment, approximately half of the poly1 layer is removed from the periphery area. Only a portion of the poly1 layer is removed because if the layer is completely removed, some of the periphery gate oxide could inadvertently be removed thereby destroying the uniformity of the periphery gate oxide. Finally, thereafter a type-2 layer of polysilicon (poly2) is deposited in all areas, via step 212.

Figure 4 is an exploded view of Figure 3(g) illustrating a cross sectional view of a flash memory device in accordance with present invention showing both the core and periphery areas. The periphery area comprises a periphery poly1 layer 302 directly underneath a poly2 layer 304 wherein the periphery poly1 layer 302 is approximately half the height of the core poly1 layer 306.

The method for fabricating the flash memory device as described herein results in a significant improvement in the reliability of the flash memory device, as well as the periphery transistors.

A flash memory device and a method of fabrication thereof has been disclosed. Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present

invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

0941370 082801